**Lab Experiment 9**

**Design and Analysis of CMOS inverter using LTSPICE**

**9.1 Objective:** To learn the design of CMOS inverter in circuit level and get the spice netlist using LTSPICE tool.

# **9.2 Software tools Requirement**

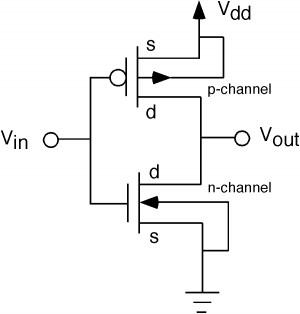
LTSPICE software

# **9.3 Prelab Questions**

1. What are the advantages of SPICE software?
2. What are the differences between enhancement and depletion mode transistors?
3. What is the difference between strong 1 and weak 1?
4. What is meant by transistor sizing?

**9.4 Problem 1: Design and analyze the CMOS inverter in circuit level, verify the transfer characteristics and infer the SPICE netlist using LTSPICE.**

## **9.4.1 Logic Diagram**



**Schematic Diagram:**

**Output Waveform:**

**Net list :**

# **9.5 Post lab**

1. Perform DC Analysis for CMOS Inverter in LTSPICE.

**9.6 Result:**

Thus, the design and analyse of CMOS Inverter has been performed, transfer characteristics have been verified using LTSPICE tool.

# **Lab Experiment 10**

**Design and Analysis of Complex CMOS gates and Pseudo NMOS gates using LTSPICE**

**9.1 Objective:** To learn the design of Complex CMOS gates and Pseudo NMOS gates in circuit level and get the spice net list using LTSPICE tool.

**9.2 Software tools Requirement**

LTSPICE software

**9.3 Prelab Questions**

1. What is meant by Pseudo NMOS logic?
2. What are the advantages and drawbacks of Pseudo NMOS?
3. In Pseudo NMOS logic, PMOS transistor operates in **resistive region**.
4. What is meant by body effect?
5. What are the different types of operating region in MOSFET?

**9.4 Problem 1: Design and analyse the Complex CMOS gate in circuit level, verify the transfer characteristics and infer the SPICE netlist using LTSPICE.**

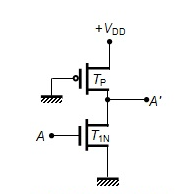
**9.4.1 Problems:**

**1. complex CMOS logic for OUT= ~(A+BC)**

**9.4.3 Output of complex CMOS logic for OUT= ~(A+BC)**

**9.4.4 SPICE NETLIST:**

**9.4.5 Pseudo NMOS gate Inverter:**



**9.4.6 Pseudo NMOS Inverter output:**

**9.4.7 SPICE NET LIST :**

**9.5 Post lab:**

1. Design Complex CMOS logic Out= ~(AB+CD) in LTSPICE.
2. Design Pseudo NMOS NAND gate in LTSPICE.

**9.6 Result:**

Thus, the design and analyze of Complex CMOS gate and Pseudo NMOS gate have been performed and its transfer characteristics is verified using LTSPICE tool.

**LAB EXPERIMENT – 10**

**Design and Analysis of Differential Cascode Voltage Switch Logic (DCVSL), Pass transistor logic and Complementary Pass Transistor** **Logic using LTSPICE/HSPICE**

**10.1 Objective:** Design and Analysis of Differential Cascode Voltage Switch Logic (DCVSL), Pass transistor logic and Complementary Pass Transistor Logic using LTSPICE/HSPICE

**10.2 Software tools Requirement Equipment’s:**

LTSPICE/HSPICE software

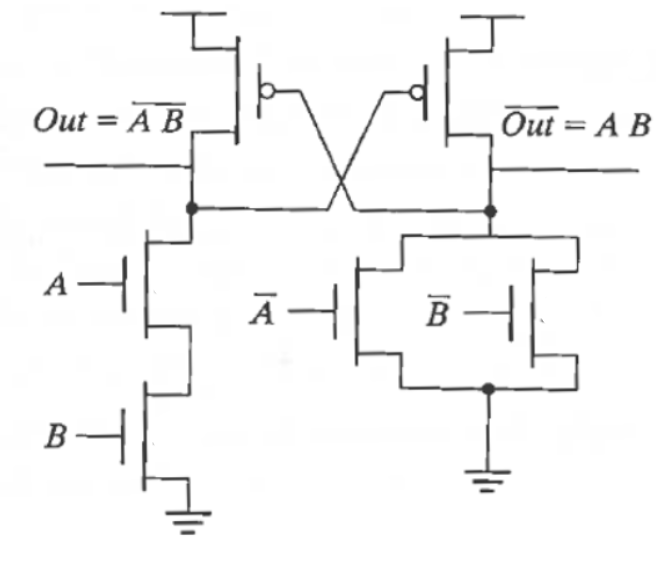
**10.3 Prelab Questions:**

1. Differentiate Dynamic and Domino CMOS logic

2. Explain Domino CMOS logic with an example

**Problem 10.4.1:** Design and analyse Differential Cascode Voltage Switch Logic (DCVSL) using LTSPICE/HSPICE

**Circuit Diagram**



**Figure 10.4.1 Differential Cascode Voltage Switch Logic (DCVSL**)

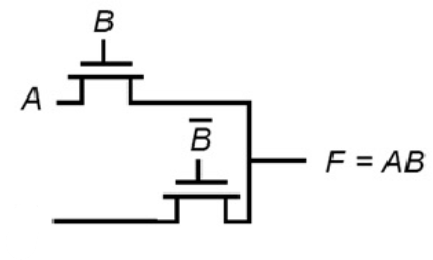
**Program:-**

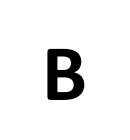
.

**Output:**

**Problem 10.4.2:** Design and analyze the Pass transistor Logic for a 2 input AND Gate in circuit level, verify the characteristics using LTSPICE/HSPICE

**Circuit Diagram:**



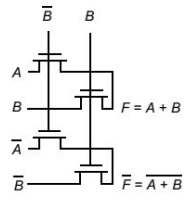


**Figure 10.4.2 Two input AND Gate Pass transistor Logic**

**Program:-**

**Output:**

**Problem 10.4.3 : Design and analyze the complementary Pass transistor Logic for a 2 input OR/NOR in circuit level, verify the characteristics using LTSPICE/HSPICE.**

****

**Figure 10.4.3 Two input OR/NOR Complementary Pass Transistor Logic**

**Program:**

**OUTPUT:**

**10.5 Post lab:**

Design and analyze the Pass transistor Logic for a 2 input XOR in circuit level, verify the characteristics using LTSPICE/HSPICE

**10.6 Result:**

Thus DCVSL, CPL and Pass Transistor Logic is successfully designed, code were written and graphs are verified using LTSPICE/HSPICE.

**LAB EXPERIMENT - 11**

**N- Input Dynamic NAND gate**

**11.1 Objective:** To study and design the two input dynamic NAND gate using LTSPICE/HSPICE and verify the simulation result.

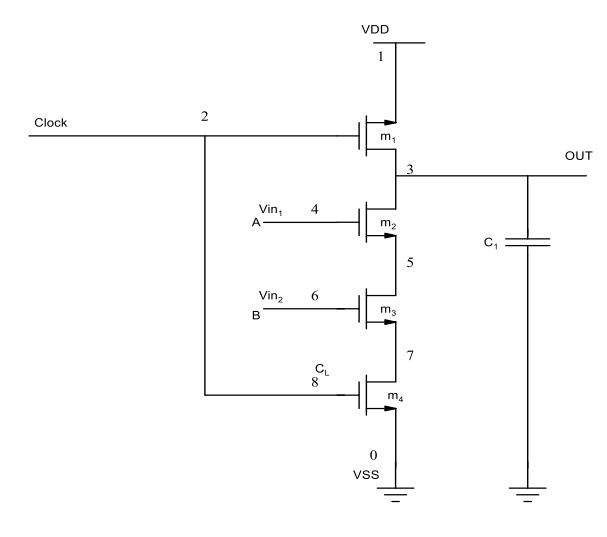
**11.2 Software required: LTSPICE/**HSPICE

**11.3** **Pre-lab Questions**

1. Differentiate static and dynamic CMOS logic.

2. Explain NORA CMOS logic.

**11.4 Circuit Diagram :**

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**Figure 11.1 Two input dynamic NAND gate**

**11.5 Program:**

**11.6 Output:**

* 1. **Post Lab Questions:**

1.Realize the n-type dynamic NOR gate using the LTSPICE/HSPICE.

**11.8 Result:**

Thus the design of two input dynamic NAND gate, MOS transistor level using LTSPICE/HSPICE was studied and simulated.